FIG 1 Prior Art

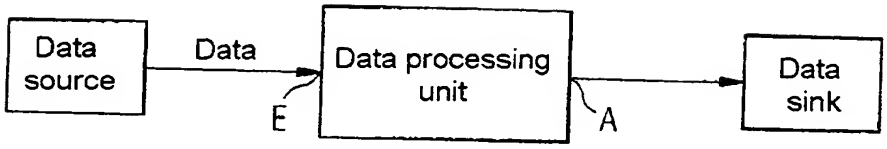


FIG 2 Prior Art

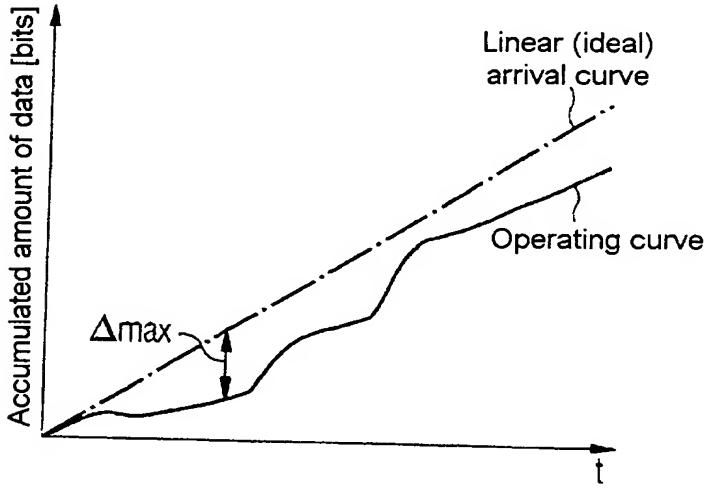


FIG 3 Prior Art

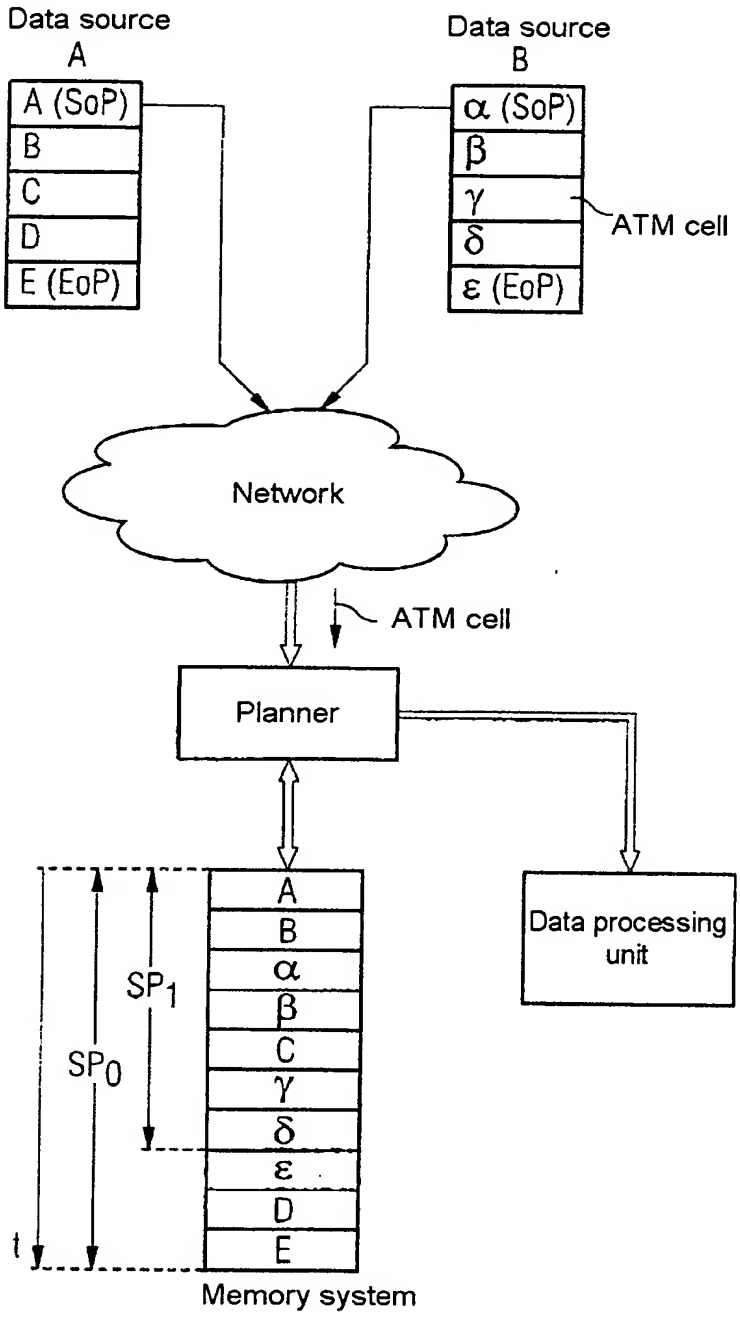


FIG 4 Prior Art

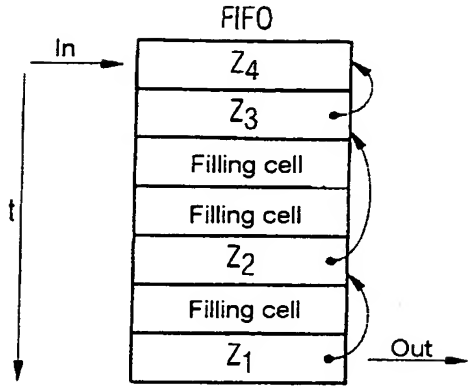
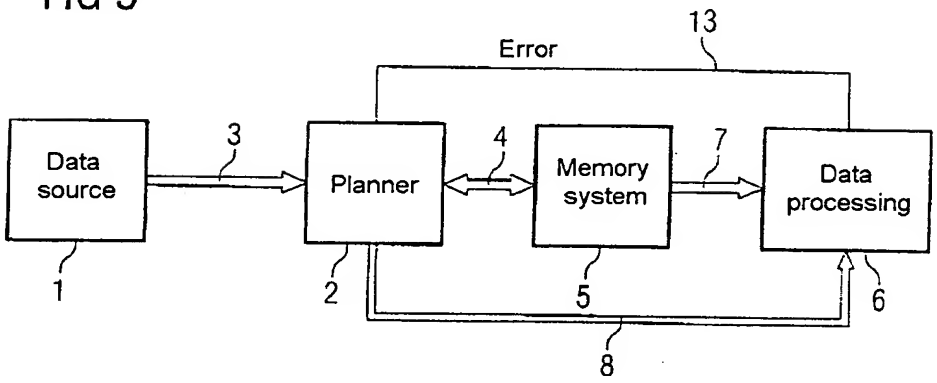


FIG 5



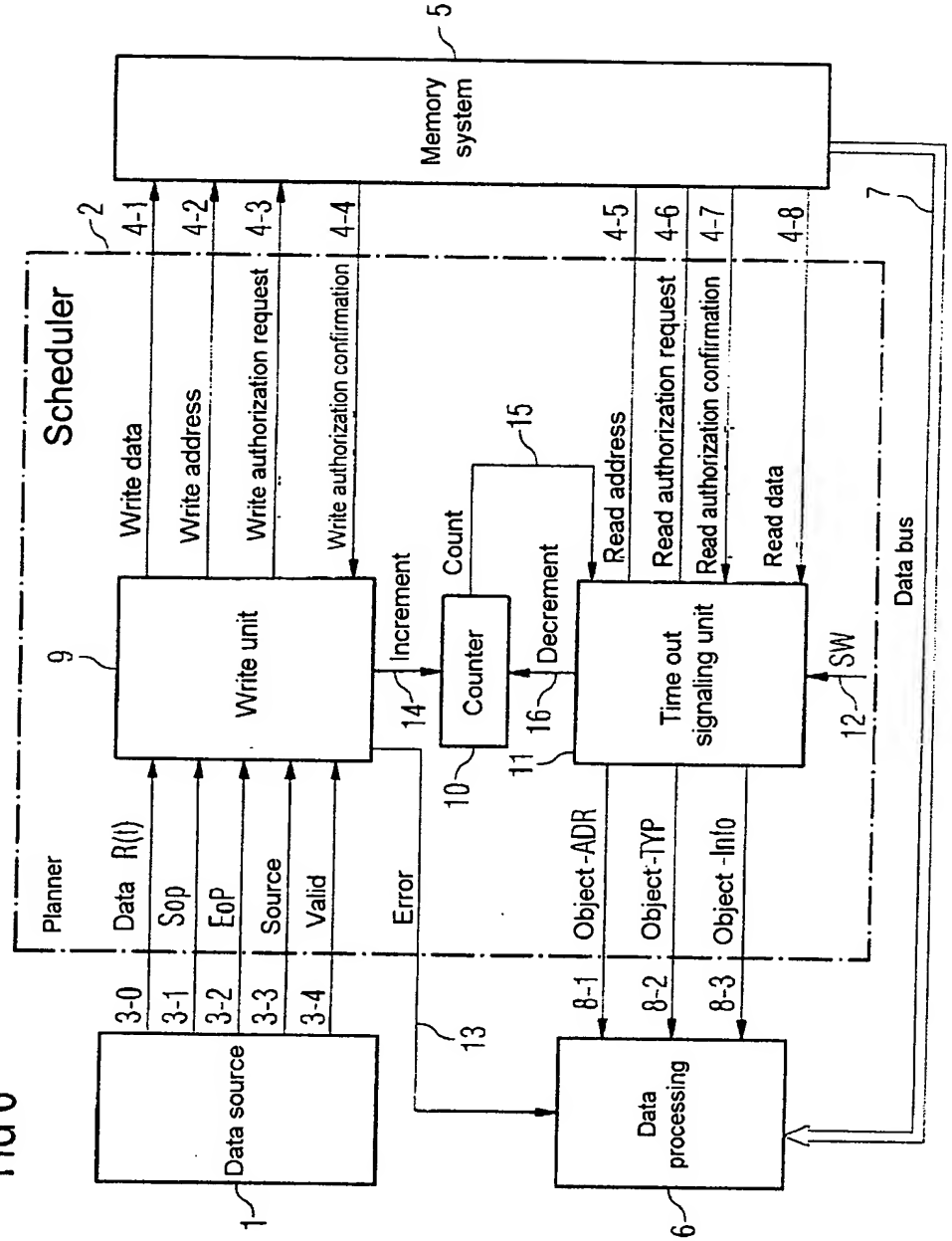

Memory system
5
Scheduler
2
Write data
Write address
Write authorization request
Write authorization confirmation
4-1
4-2
4-3
4-4
4-5
4-6
4-7
4-8
7
Data bus
Read address
Read authorization request
Read authorization confirmation
Read data
9
Write unit
Increment
Count
15
Counter
Decrement
14
16
10
11
Time out signaling unit
SW
12
Planner
Data R(l)
Sop
EoP
Source
Valid
Error
Object-ADR
Object-TYP
Object-Info
3-0
3-1
3-2
3-3
3-4
8-1
8-2
8-3
13
Data source
1
Data processing
6

FIG 6

FIG 7

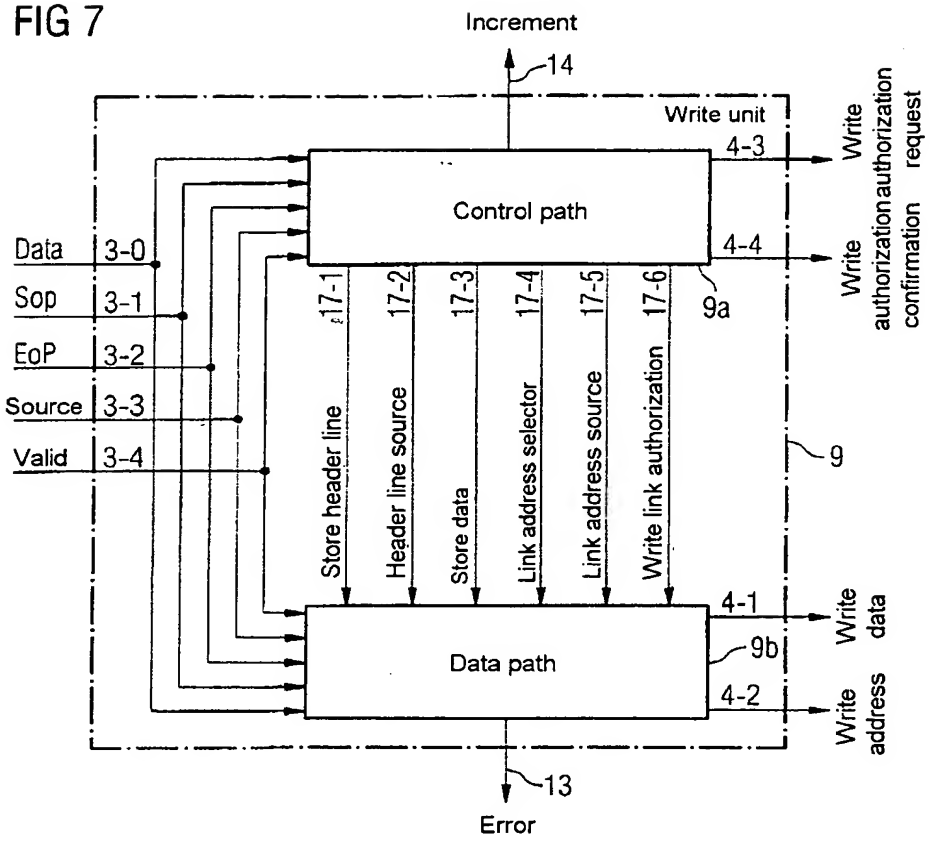

Increment
14
Write unit
4-3
Write authorization request
Control path
4-4
Write authorization confirmation
Data
3-0
Sop
3-1
EoP
3-2
Source
3-3
Valid
3-4
17-1
17-2
17-3
17-4
17-5
17-6
9a
Store header line
Header line source
Store data
Link address selector
Link address source
Write link authorization
9
4-1
Write data
9b
Data path
4-2
Write address
13
Error

FIG 8

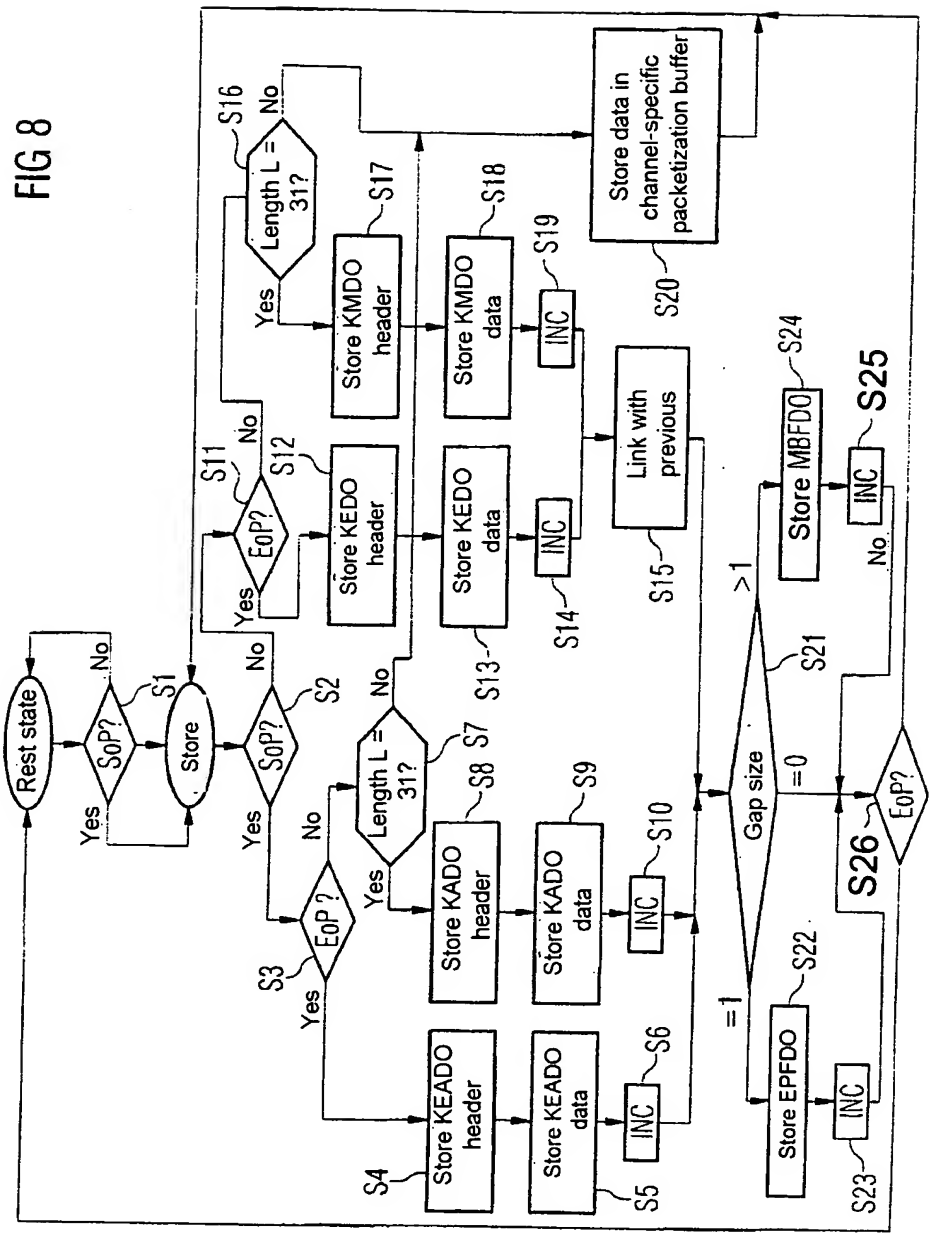

Rest state
SoP?
No
Yes
S1
Store
SoP?
No
Yes
S2
EoP?
No
Yes
S3
Store KEADO header
S4
Store KEADO data
S5
INC
S6
Length L = 31?
No
Yes
S7
Store KADO header
S8
Store KADO data
S9
INC
S10
EoP?
No
Yes
S11
Store KEDO header
S12
Store KEDO data
S13
INC
S14
Link with previous
S15
Length L = 31?
No
Yes
S16
Store KMDO header
S17
Store KMDO data
S18
INC
S19
Store data in channel-specific packetization buffer
S20
Gap size
=1
>1
=0
S21
Store EPFDO
S22
INC
S23
Store MBFDO
S24
INC
S25
EoP?
S26

FIG 9

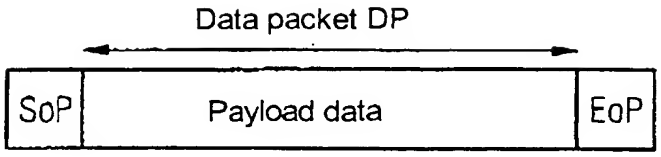

Data packet DP
SoP
Payload data
EoP

FIG 10

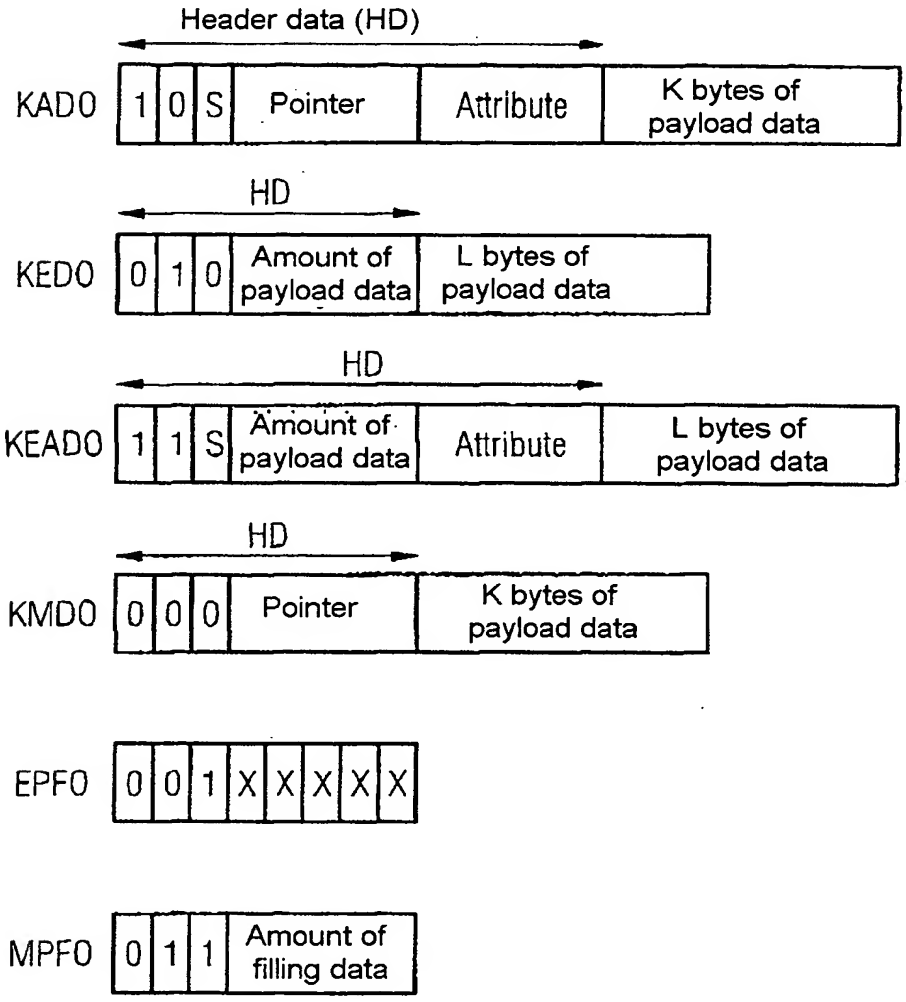

Header data (HD)
KADO
1
0
S
Pointer
Attribute
K bytes of payload data
HD
KEDO
0
1
0
Amount of payload data
L bytes of payload data
HD
KEADO
1
1
S
Amount of payload data
Attribute
L bytes of payload data
HD
KMDO
0
0
0
Pointer
K bytes of payload data
EPFO
0
0
1
X
X
X
X
X
MPFO
0
1
1
Amount of filling data

FIG 11

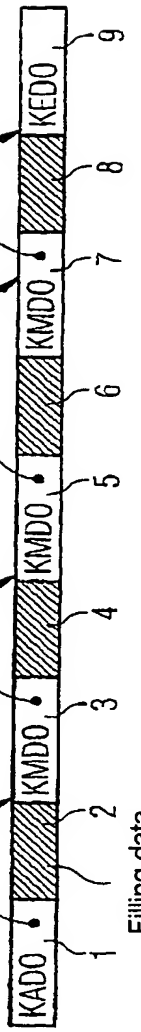

KADO
KMDO
KMDO
KMDO
KEDO
1
2
3
4
5
6
7
8
9
Filling data

FIG 12

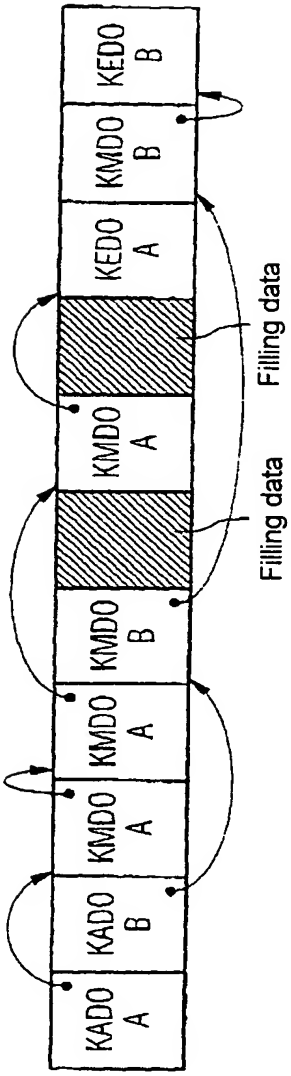

KADO A
KADO B
KMDO A
KMDO A
KMDO B
KMDO A
KEDO A
KMDO B
KEDO B
Filling data
Filling data

FIG 13A

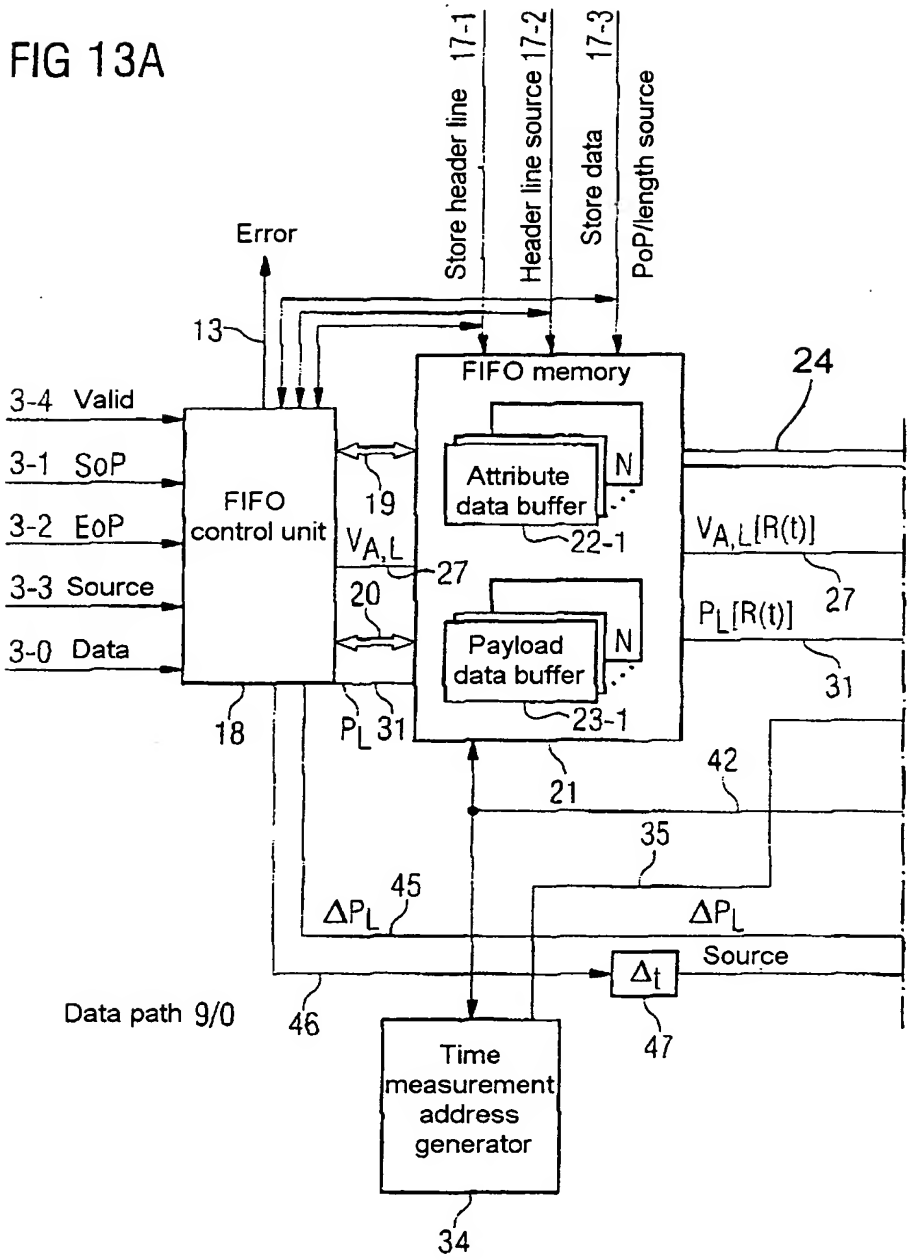

Store header line 17-1
Header line source 17-2
Store data 17-3
PoP/length source
Error
13
FIFO memory
24
3-4 Valid
3-1 SoP
3-2 EoP
3-3 Source
3-0 Data
FIFO control unit
19
$V_{A,L}$
27
20
Attribute data buffer
N
22-1
Payload data buffer
N
23-1
$V_{A,L}[R(t)]$
27
$P_L[R(t)]$
31
18
P_L 31
21
42
35
45
ΔP_L
ΔP_L
Source
Δ_t
47
Data path 9/0
46
Time measurement address generator
34

FIG 13B

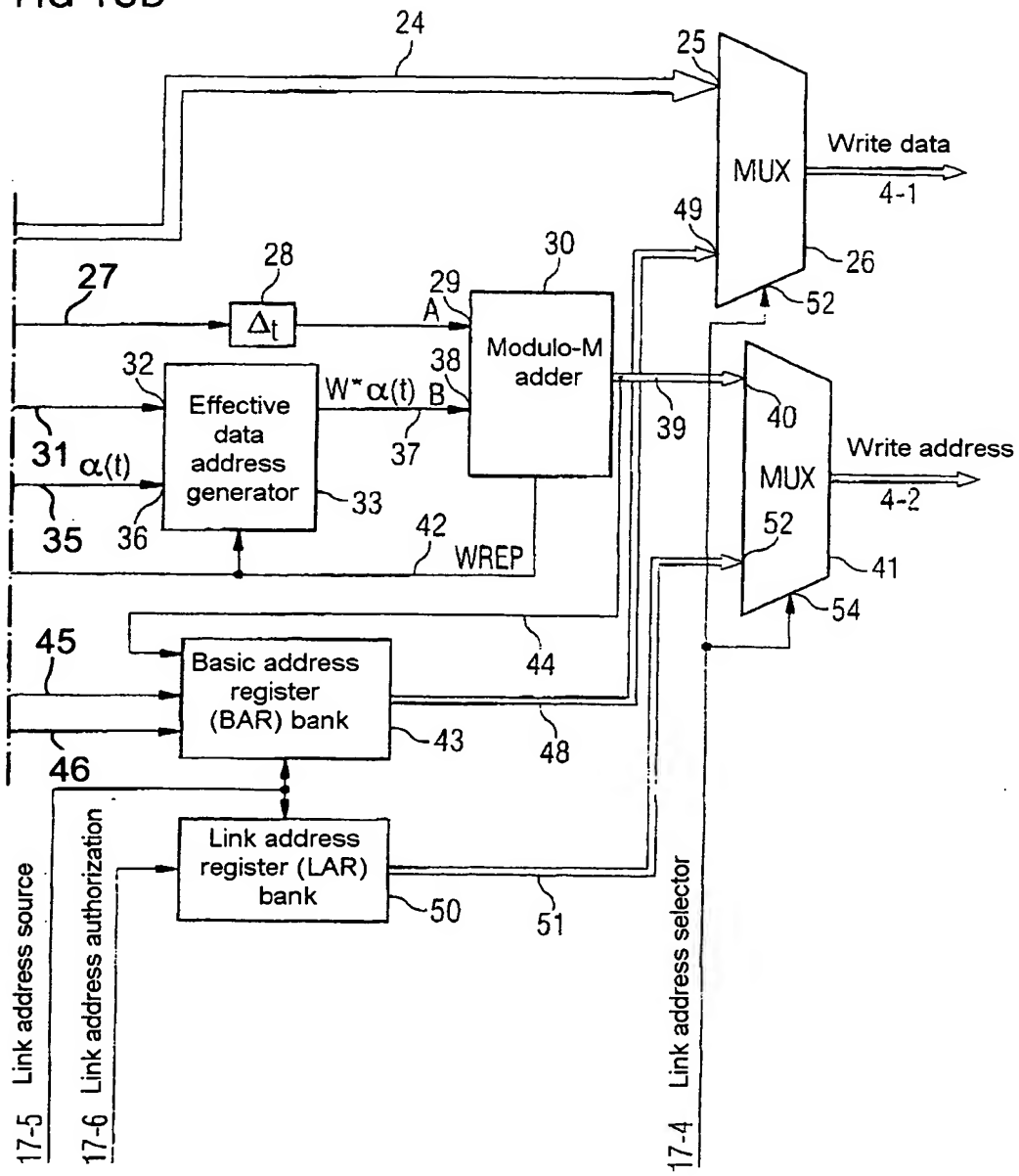

24
25
MUX
Write data
4-1
49
26
52
27
28
30
29
A
Modulo-M adder
Δ_t
32
38
W*α(t)
B
Effective data address generator
39
40
Write address
4-2
31
α(t)
37
MUX
52
35
36
33
42
WREP
41
54
45
44
Basic address register (BAR) bank
43
48
46
Link address register (LAR) bank
50
51
17-5 Link address source
17-6 Link address authorization
17-4 Link address selector

FIG 14

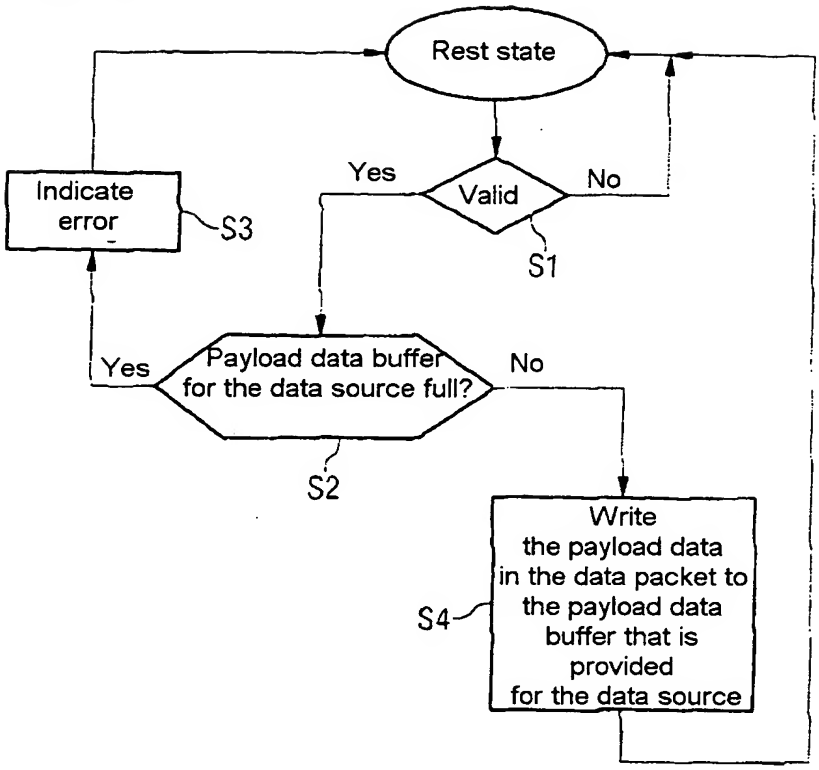

Rest state
Valid
Yes
No
S1
Indicate error
S3
Payload data buffer for the data source full?
Yes
No
S2
Write the payload data in the data packet to the payload data buffer that is provided for the data source
S4

FIG 15

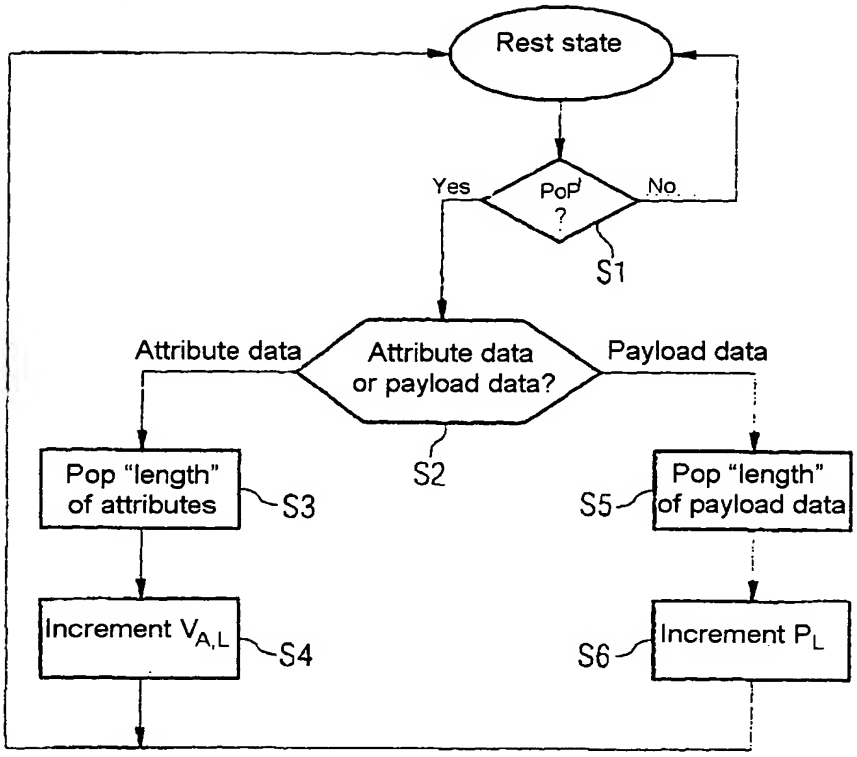
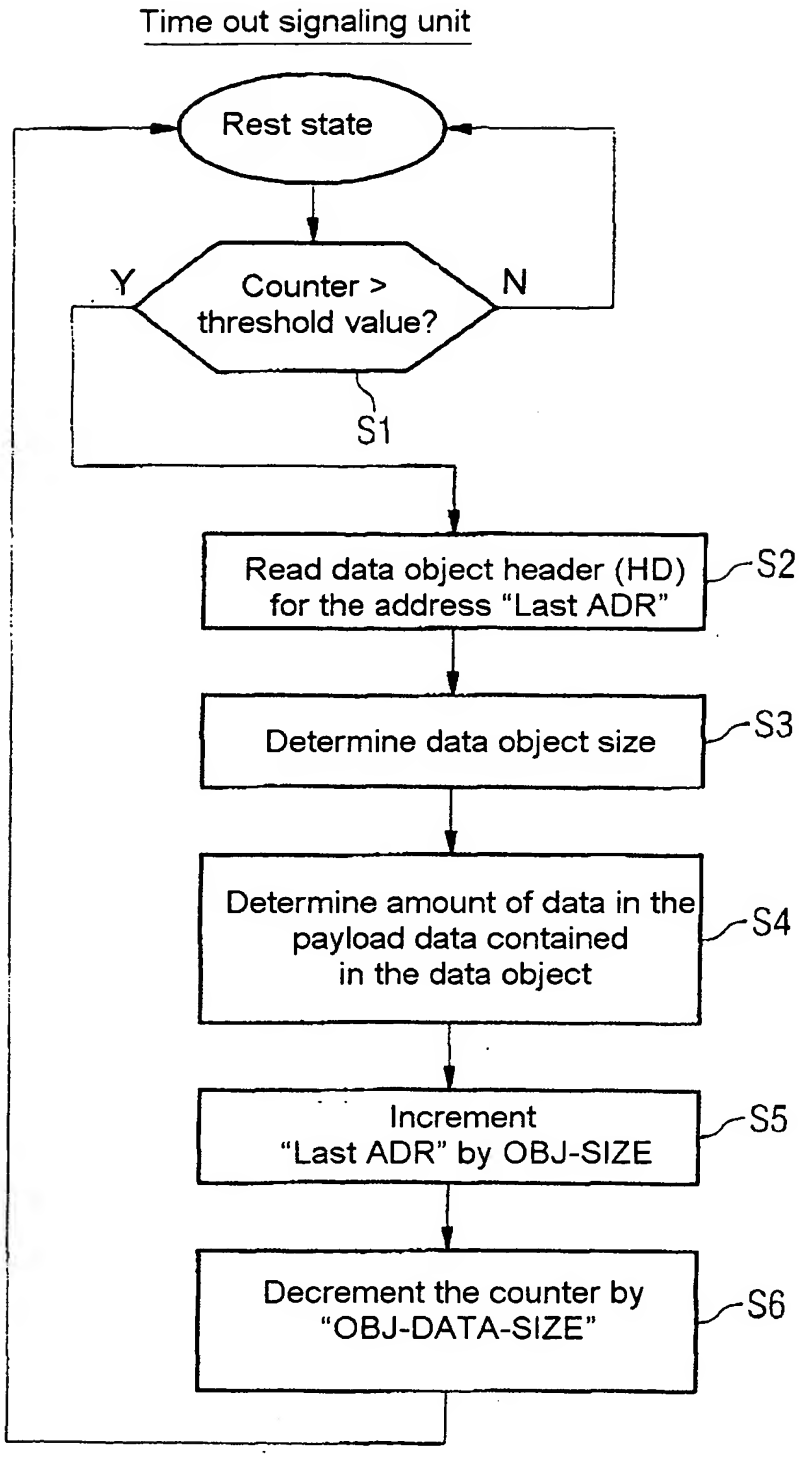

Rest state
Yes
Pop ?
No
S1
Attribute data
Attribute data or payload data?
Payload data
S2
Pop "length" of attributes
S3
Pop "length" of payload data
S5
Increment $V_{A,L}$
S4
Increment P_L
S6

FIG 16


Time out signaling unit
Rest state
Y
Counter > threshold value?
N
S1
Read data object header (HD) for the address "Last ADR"
S2
Determine data object size
S3
Determine amount of data in the payload data contained in the data object
S4
Increment "Last ADR" by OBJ-SIZE
S5
Decrement the counter by "OBJ-DATA-SIZE"
S6